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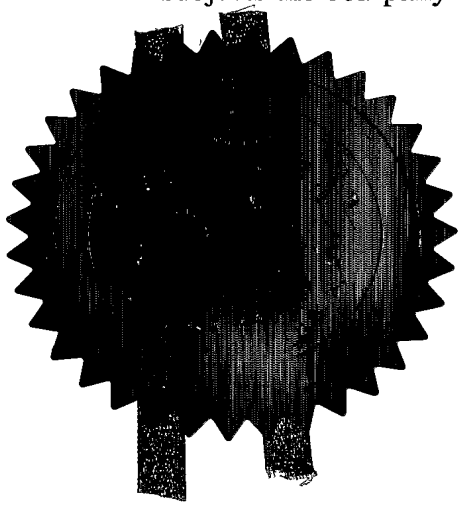

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Dated 5 January 2005

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The **Patent Office**

1/77

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1. Your reference — JPP236

2. Patent application number *(The Patent Office will fill in this part)* — 0329351.1 — 18 DEC 2003

3. Full name, address and postcode of the or of each applicant *(underline all surnames)*

Andrew Holland
9 Cromwell Place
London
SW14 7HA

Patents ADP number *(if you know it)* 8775009001

If the applicant is a corporate body, give the country/state of its incorporation

4. Title of the invention — IMPROVEMENTS IN OR RELATING TO ELECTRONICS PACKAGING

5. Name of your agent *(if you have one)* — Barker Brettell

"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*

10-12 Priests Bridge
London
SW15 5JE

Patents ADP number *(if you know it)* 7442494003

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Country	Priority application number *(if you know it)*	Date of Filing *(day/month/year)*

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Statement of inventorship and right to grant of a patent *(Patents Form 7/77)*	
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Request for substantive examination *(Patents Form 10/77)*	
Any other documents *(please specify)*	

11. I/We request the grant of a patent on the basis of this application.

Signature: Barker Brettell — Date: 18 December 2003

12. Name and daytime telephone number of person to contact in the United Kingdom: James P. Peel — Tel: 020 8392 2234

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IMPROVEMENTS IN OR RELATING TO ELECTRONICS PACKAGING

The present invention relates to semiconductor packages, mounting assemblies therefor and a method of manufacture, and more particularly but not limited to, micro mounting packages that have a simple integrated heatsink and electromagnetic shield.

The objective of any electronics package is to protect sensitive integrated circuits from harsh environments without inhibiting electrical performance. The package is used to electrically and mechanically attach a chip to an intended device. One popular family of electronics package is the Micro Leadframe Packaging (MLP). MLP is based upon a patterned and etched metal mounting commonly with a central pad, onto which a single or multiple semiconductor chips or dies are mounted, connected with wirebonds to isolated package pins, then encapsulated in a plastic sealing material. A sealing material is applied around the metal of the mounting and the integrated circuit with wirebonds to form a hard, protective plastic body.

Further information relative to mounting technology may be found in Chapter 8 of the book Micro Electronics Packaging Handbook, (1989), edited by R.Tummala and E.Rymaszewski, incorporated by reference herein. This book is published by Van Nostrand Reinhold, 115 Fifth Avenue, New York, N.Y.

Generally, manufacture is completed using an array of multiple MLP mountings. After encapsulation a mounting is separated from any supporting peripheral mounting structures and neighbouring packages by a punch or a saw.

It may be stated generally that there is a desire in the electronics packaging industry to reduce size and cost whilst at the same time as integrating more functionality. One proven route to increase functionality is to include several integrated circuits in the same MLP. Modern assembly techniques allow dies to be stacked or flip mounted (i.e. mounted in an inverted orientation), ensuring a minimal final package size.

There are additional problems to be solved in the electronics packaging industry. One such problem is that many types of integrated circuit produce high levels of unwanted thermal energy, even when in normal operation. These circuits still require integration. Thermal design is also important and a method of dissipating heat to maintain electrical and mechanical stability has been sought.

Another such problem is that many electronics products need to operate in an electrically noisy environment. A method of protecting a sensitive integrated circuit within the package from unwanted electrical interference has also been sought.

A further such problem is that many electronics products require direct electrical connection to the system ground potential to obtain optimum performance. If this connection is electrically impaired (e.g. by resistive or inductive impairment) many integrated circuits particularly operating at intermediate and high frequencies or with high electrical currents may be adversely affected. A method of providing a low resistance, low inductance path to system ground has been sought.

SUMMARY OF THE INVENTION

The present invention relates to a semiconductor package, a mounting assembly therefor and a method of manufacture, and more particularly but

not limited to, a micro mounting package that has an integrated heatsink and electromagnetic shield.

According to the invention there is provided a mounting for a printed circuit board which mounting is suitable for receiving a semiconductor assembly wherein the mounting comprises:

a base support having a semiconductor assembly facing surface, and an opposed printed surface board facing surface;

a cover having a semiconductor assembly facing surface, an opposed heat radiating surface;

a connecting formation which joins the cover to the base support and provides thermal communication between the cover and the base support wherein the connecting formation has a semiconductor assembly facing surface, an opposed surface and a thickness between the two surfaces; and

a plurality of package connectors extending from the base support each of which package connectors have a printed surface board facing surface.

According to the invention there is also provided a mounting array comprising a plurality of mountings each according to the invention.

A semiconductor package comprising a semiconductor assembly having one or more semiconductor chips, which assembly is mounted on a mounting according to the invention wherein the package connectors of the mounting are in a spaced relationship with the base support and are linked electrically with the semiconductor assembly and the cover is arranged to be in a spaced parallel relationship with the base support.

The cover of the mounting is arranged to be mechanically and electrically connected to the base support and the base support is normally connected

to System Ground potential (GND) on the final product printed circuit board. The particularly advantageous feature of the present invention is the cover which provides three functions (a) a simple heatsink (b) a low resistance, low inductive path to electrical Ground (GND) and (c) to act as a local electromagnetic shield protecting sensitive functions within, or without, from unwanted electromagnetic interference.

The new package can be used for single or multiple chip. Where multiple chips are integrated it is often beneficial to "flip" smaller (daughter) chip onto a larger (mother) die. The new package facilitates connection to a simple heatsink and electromagnetic shield and System Ground (GND). Through modern assembly techniques the present invention reduces cost and area usage on a printed circuit board whilst improving thermal and electrical performance.

The connecting formation of the mounting according to the invention is preferably provided with folding means to enable the connecting formation to be bent such that the cover can be arranged to be in a spaced parallel relationship to the base support. The folding means is preferably a scored line or an etched line in the connecting formation having a thickness which is less than that of the rest of the connecting formation.

The mounting is preferably formed from a single sheet of electrically and thermally conducting material which is preferably a metal, more preferably copper.

In the package according to the invention, the semiconductor assembly is preferably attached to the base support and/or the cover. Where the assembly comprises two or more semiconductor chips, it is preferably attached to the base support and the cover. This enables a daughter semiconductor chip to be connected more directly to system ground. The

assembly is preferably electrically attached to the base support and/or cover, more preferably by conductive wire or conductive epoxy or solder material.

The package according to the invention preferably further comprises a sealing material at least partially encapsulating the mounting and the assembly such that the printed surface board facing surfaces of the package connectors and base support and the heat radiating surface of the cover are not covered by the sealing material. This is in order to protect and support the contents of the package.

The invention is illustrated with reference to the following Figures of the drawings wherein:

Figure 1 shows a side elevation, cross-sectional view of a known MLP-type semiconductor package;

Figure 2 shows a side elevation, cross-sectional view of an MLP-type semiconductor package according to the invention with a formed upper pad;

Figure 3 shows a top plan view of an MLP-type semiconductor package according to the invention;

Figure 4 shows a bottom plan view of an MLP-type semiconductor package according to the invention;

Figure 5 shows a plan view of a known MLP-type semiconductor mounting;

Figure 6 shows a plan view of an MLP-type semiconductor mounting according to the invention, laid flat and showing formed upper pad prior to bend;

Figure 7 shows a plan view of a manufacturing array of mountings according to the present invention;

Figure 8 shows a plan view of a laid flat MLP-type semiconductor mounting according to the present invention wherein the mounting has no package connectors on the edge adjacent the cover to maximise the area of the connecting formation;

Figure 9 shows a plan view of a laid flat MLP-type semiconductor mounting according to the present invention having a cover which is defined with apertures;

Figure 10 shows a plan view of a laid flat MLP-type semiconductor mounting according to the present invention having four package connectors on the side adjacent the cover;

Figure 11 shows a side elevation, cross-sectional view of a second embodiment of a semiconductor package according to the present invention;

Figure 12 shows a side elevation, cross-sectional view of a third embodiment of a semiconductor package constructed in accordance with the principles of the present invention;

Figure 13 shows a side elevation, cross-sectional view of the construction of a single bend point;

Figure 14 shows how a pair of bend points may be used to construct the connecting formation used in the present invention; and

Figure 15 shows a side-elevation, cross-sectional view of the second embodiment of the present invention mounted on a printed circuit board.

Before discussing the embodiments of the present invention, the prior art MLF-type semiconductor package is discussed below in order to provide background information regarding the techniques of construction of MLF-type semiconductor packaging.

In reference to Figure 1, there is shown a side-elevation, cross-sectional view of a known MLF-type semiconductor package 40. The semiconductor package contains a mounting 47 consisting of a base support (also referred to as a paddle or base mounting pad) 42, a plurality of package connectors (also referred to as package pins) 44, a single semiconductor chip 41 connected to the base 42 by bonding layer 48 and a plurality of wires (also referred to as wirebonds) 43 which link the chip 41 to the package connectors 44. The complete assembly is enclosed in a nonconductive sealing material 45. Sealing material 45 may be a thermoplastic or thermoset resin (including an epoxy, phenolic and/or silicone resin).

Numerous techniques for secure attachment of a semiconductor chip 41 to the base 42 are in practice, including conductive and/or nonconductive epoxy or solder 48. The top surface of the semiconductor chip 41, usually has, at its periphery, a plurality of connecting pads 46. A plurality of package connectors 44 surround the mounted semiconductor chip 41 and base 42. Wires 43 electrically connect to the semiconductor die

connecting pads 46 and the package connectors 44. Package connectors 44 are rectangular in cross-section but may be etched to improve fixing to sealing material 45. The pluralities of package connectors 44 are located at the periphery of the semiconductor package 40. The base support 42 is generally located centrally to the package base. Package connectors 44 and base support 42 are used to connect to a printed circuit board (PCB), not shown.

An MLF-type semiconductor package aids dissipation of heat generated from the operation of the semiconductor chip 41 via the lower exposed surface of the base support 42 and the lower and lateral exposed surfaces of the package connectors 44. Some heat is also dissipated from the upper surface, to air surrounding the semiconductor package 40. However the sealing material 45 tends to prevent this by insulating the semiconductor chip 41.

Semiconductor chips 41 are designed for many different applications and markets. Often there is an advantage in providing an electromagnetic shield over and in close proximity to the semiconductor chip 41. Such a shield may protect the semiconductor chip from unwanted interference from external radio signals and propagated waves but also protect the external system from signals generated from semiconductor chip 41 under its own operation.

The prior art package has no externally exposed top metal pad to aid additional thermal dissipation or to give electromagnetic shielding protection to the semiconductor chip 41 or external system by presenting a shield or barrier to radio signals. The prior art package does not allow direct connection to the rear face of a stacked (flip-chip) mounted daughter die when mounted to the upper surface of the semiconductor die 41 on the base 42.

Figures 2 to 4 and 6 to 14 illustrate aspects of the invention. In these Figures, like features are indicated by like identification numbers.

Referring to Figure 2, here shown is a side-elevation, cross-sectional view of semiconductor package 50. This is the first embodiment of a semiconductor package according to the present invention. The semiconductor package contains a mounting 57 consisting of a base support 52, a cover 60, connecting formation 59, a plurality of package connectors 54, a single semiconductor chip 51 and a plurality of wires 53. The complete assembly is enclosed in a nonconductive sealing material 55. Sealing material 55 may be a thermoplastic or thermoset resin (including an epoxy, phenolic and/or silicone resin). Figure 2 shows a semiconductor chip 51 mounted to the base support 52. Numerous techniques of secure attachment are in practice, including conductive and nonconductive epoxies, or solder 58. The top surface of the semiconductor chip 51, usually has, at its periphery, a plurality of connecting pads 56. A plurality of package connectors 54 surround the mounted semiconductor chip 51 and base support 52. Wires 53 electrically connect to the semiconductor die connecting pads 56 and the package connectors 54. The pluralities of package connectors 54 are located at the periphery of the semiconductor package 50. The base support 52 is generally located centrally to the package base. Package connectors 54 and base support 52 are used to connect to a printed circuit board (not shown).

The connecting formation 59 connects the base support 52 and cover 60. The connecting formation 59 provides a low resistance, low inductance thermally efficient path from the cover 60 to the base mounting pad 52 and to the external printed circuit board (not shown). The base support 52 and cover 60, the connecting formation 59 and package connectors 54

are secured to a mounting foil via mounting supporting structures or tie-bars (not shown). Tie bars and other supporting structures are trimmed off at the package dicing stage of manufacture.

The mounting 57 may be etched to provide additional locking strength between the mounting 57 and the sealing material 55. The connecting formation 59 has a lateral etch, cut or scribe used at each end of the connecting formation 59 to define bend points 70 for the formation of the cover 60 of the package. The top side of the base support 52 is attached to the semiconductor chip while the bottom side of the base mounting pad 52 is exposed to the outside of the semiconductor package 50. The bottom side of the base support 52 and the upper side of the cover 60 are electroplated with a corrosion-minimizing material such as tin, gold, tin lead, tin bismuth, nickel palladium or other suitable alloy. The bottom side of the base support 52 will be mounted to the printed circuit board (not shown). The topside of the cover 60 is exposed to the outside of the semiconductor package 50 and is generally centrally located in the top surface of the package.

The mounting 57 is fabricated from an electrically and heat conducting material such as copper. Heat generated from the operation of the semiconductor chip 51 is dissipated throughout the semiconductor package and through the bottom of the base mounting pad 52 to the printed circuit board. The exposed cover 60 will aid heat dissipation. Heat will also be dissipated through the plurality of package connectors 54. The plurality of package connectors 54 does not normally touch the base mounting pad 52.

Still referring to Figure 2, semiconductor package 50 has a semiconductor chip 51 attached to the base support 52 via an adhesive or suitable solder material 58. The plurality of package connectors 54 electrically connect to the semiconductor chip 51 through a plurality of wires 53. Each wire

53 has a first end electrically connected to one of the bond pads 56 on the top side of the semiconductor chip 51 and a second end connected to the lower portion of one of the package connectors 54. Wires can be made of any electrically conductive material; gold aluminium or silver are common choices.

Sealing material 55 preserves the spatial relationship between the cover 60 and the base support 52, the connecting formation 59, wires 53, mounted semiconductor chip 51, and semiconductor package connectors 54. The sealing material 55 forms a rigid structure to maintain protection and form to the semiconductor package 50 and its component parts. After sealing only the plated areas of the base support 52 and cover 60, lower and outer edges of the package pins 54 remain exposed allowing connection to a printed circuit board.

Figure 3 shows a top plan view of semiconductor package 50. The cover 60 is located generally to the middle of the semiconductor package 50. At the four edges of the semiconductor package 50 sealing material 55 is shown defining the outer edge. The sealing material 55 ensures an interlocking structure with the cover 60. Only the upper portion of the cover 60 is exposed.

Figure 4 shows a bottom plan view of the semiconductor package 50. As shown the base support 52 is located, generally, to the middle of the semiconductor package 50, surrounded on four sides by a plurality of package connectors 54. At the four edges of the semiconductor package 50, sealing material 55 defines the outer edge. The sealing material 55 ensures an interlocking structure with the base support 52 and package connectors 54. Only the lower exposed and plated portion of the package connectors 54 and base support 52 are visible.

Figure 5 shows a plan view of a known MLP-type package 47 for a semiconductor package 40. As shown the base support 42 is located generally to the middle of the semiconductor package 40, surrounded on four sides by a plurality of package connectors 44.

Figure 6 shows a plan view of a mounting 57 for a semiconductor package 50 according to the present invention shown in its basic state prior to bending. Support structures 74 for mounting definition are shown for two pins on the package near to where the connecting formation 59 is defined. Other tie-bars and support structures for mounting manufacture are not shown, however the plurality of package connectors 54 are shown interconnected as the case may be before trimming. Etched or scribed bend points 70 (dotted) are positioned to define the connecting formation 59. A dashed line is shown intersecting each about the plurality of package connectors 54. The dashed line indicates the package outer dimension after dicing.

Figure 7 shows a plan view of an array of multiple individual mountings 57 for semiconductor package 50 to show how an individual mounting 57 may be manufactured from a larger area of metal material.

Figure 8 shows a plan view of a variation of the mounting 57 for semiconductor package 50 shown in Figure 6. In the mounting shown in Figure 8, there are no pins on side adjacent the connecting formation 59. Tie-bars and support structures for mounting manufacture are omitted, however the plurality of package connectors 54 for the other three sides are shown interconnected as the case may be before trimming.

Figure 9 shows a plan view of a variation of the mounting 57 for semiconductor package 50 shown in Figure 6. The cover 60 forms a

plurality of apertures. An example, arbitrary, pattern is shown though an alternative pattern could be used.

Figure 10 shows a plan view of a variation of the present invention mounting 57 for semiconductor package 50 shown in Figure 6. There are four pins on the package side where the connecting formation 59 is defined.

Figure 11 shows a side-elevation, cross-sectional view of a second embodiment of a semiconductor package 50 according to the invention. In this embodiment, multiple semiconductor chips are integrated. There is a single mother semiconductor chip 61 and two inverted chips 62, 63 mounted on the mother semiconductor chip 61. The larger mother semiconductor chip 61 may be mounted first to the base support 52. The top surface of the semiconductor chip 61, is specifically designed to have corresponding connection pads 64 upon which to mount a plurality of smaller daughter chips 62, 63. Modern "flip-chip" assembly techniques are used to mount the daughter chips 62, 63 upon the upper surface of the mother semiconductor chip 61.

The daughter semiconductor chips (62, 63) are pre-thinned and prefabricated, perhaps at wafer level, with materials to form a plurality of "bumps" to facilitate the flip-chip connection. Singular bumps 66 are positioned at each of the connection pads 65 of the daughter die (62, 63). Popular methods of bumping semiconductor chips are, solder deposition/ reflow or gold stud. Alternative attachment materials include an-isotropic conducting materials.

Under-fill material 67 may be added to improve reliability and thermal performance of the flip-chip bonds 66. Some types of under-fill material

67 can be applied to the flip-chip stack either before or after the placement is made.

The direct connection of electrical, and mechanical path from the daughter chips 62, 63 to the cover 60 will aid thermal and electrical performance. The exposed cover 60 will aid heat dissipation.

Figure 12 shows a side-elevation, cross-sectional view of a third embodiment of a semiconductor package 50. In this embodiment, as in the second embodiment shown in Figure 11, multiple semiconductor chips are integrated. The plurality of wires 53 in the second embodiment are replaced with through-hole vias 68 in the mother semiconductor chip 61.

The mother semiconductor chip 61 is designed with through-hole vias 68 with upper and lower capture pads 75, which facilitate a vertical connection through to the base of the chip 61. The through-hole via 68 and capture pads 75 may be designed to align and allow connection directly with the package connectors 54 and/or base support 52. Multiple through-hole vias 68 may be arrayed to improve electrical connection or thermal relief. Conductive epoxy or solder material 58 is pre-deposited upon the plurality of package connectors 54. This deposition of a conductive layer or solder 58 is made at the same time as the deposition of epoxy or solder material on the base support 52. Upon placement of the mother semiconductor chip 61 a desired electrical connection between the underside of the mother semiconductor chip 61 and package connectors 54 and/or base support 52 is formed.

Figure 13(a) shows a side-elevation, cross-sectional view of a defined bend point 70 in the mounting metal foil. Processes of etching and scribing are used to define a particular cross-section within the mounting metal foil which will provide a repeatable, reliable and robust mechanism

for bending of the mounting to form the connecting formation 59 and cover 60.

Figure 13(b) shows a side-elevation, cross-sectional view of the same single defined bend point 70 in the mounting metal foil after being formed to an angle of 90 degrees.

Figure 14(a) shows a side-elevation, cross-sectional view of two defined bend points 70 in the mounting metal foil. The bend points 70 are defined at a distance specific and relating to the desired height of connecting formation 59 and separation from base support 52 and cover 60. Processes of etching and/or scribing are used to define a particular cross-section within the mounting metal foil which will provide a repeatable, reliable and robust mechanism for bending of the mounting to form the connecting formation 59 and cover 60.

Figure 14(b) shows a side-elevation, cross-sectional view of same two defined bend points 70 in the mounting metal foil after each is formed to an angle of 90 degrees.

Figure 15 shows a side-elevation, cross-sectional view of the second embodiment of the present invention, a semiconductor package 50 mounted to a printed circuit board 73. A thermally conductive, electrically non-conductive material 71 is deposited upon the top surface (cover 60) of the package and used to dissipate heat. The thermally conductive material 71 is shown deposited so that it makes contact to a suitable casing or body 72 of the final product. Open arrows depict the general dissipation of heat energy away from the package.

CLAIMS

1. A mounting for a printed circuit board which mounting is suitable for receiving a semiconductor assembly wherein the mounting comprises:

a base support having a semiconductor assembly facing surface, and an opposed printed surface board facing surface;

a cover having a semiconductor assembly facing surface, an opposed heat radiating surface;

a connecting formation which joins the cover to the base support and provides electrical and thermal communication between the cover and the base support wherein the connecting formation has a semiconductor assembly facing surface, an opposed surface and a thickness between the two surfaces; and

a plurality of package connectors extending from the base support each of which package connectors have a printed surface board facing surface.

2. A mounting as defined in claim 1 wherein the connecting formation is provided with folding means to enable the connecting formation to be bent such that the cover can be arranged to be in a spaced parallel relationship to the base support.

3. A mounting as defined in claim 2 wherein the folding means is a scored line and/or an etched line in the connecting formation having a thickness which is less than that of the rest of the connecting formation.

4. A mounting as defined in any one of the preceding claims which is formed from a single sheet of electrically and thermally conducting material.

5. A mounting as defined in claim 4 wherein the conducting material is metal, preferably copper.

6. A mounting substantially as hereinbefore described above and/or as illustrated with reference to Figures 6 and 8 to 10 of the accompanying drawings.

7. A mounting array comprising a plurality of mountings each as defined in any one of the preceding claims.

8. A semiconductor package comprising a semiconductor assembly having one or more semiconductor chips, which assembly is mounted on a mounting as defined in any one of claims 1 to 6 wherein the package connectors of the mounting are in a spaced relationship with the base support and are linked electrically with the semiconductor assembly and the cover is arranged to be in a spaced parallel relationship with the base support.

9. A semiconductor package as defined in claim 8 wherein the assembly is attached to the base support and/or the cover.

10. A semiconductor package as defined in claim 9 wherein the assembly comprises two or more semiconductor chips and is attached to the base support and the cover.

11. A package as defined in any one of claims 8 to 10 which further comprises a sealing material at least partially encapsulating the mounting and the assembly such that the printed surface board facing surfaces of the package connectors and the base support and the heat radiating surface of the cover are not covered by the sealing material.

12. A package as defined in any one of claims 8 to 11 wherein the assembly is electrically connected to the base support and/or cover.

13. A package as defined in claim 12 wherein the assembly is electrically connected by conductive wire or conductive epoxy or solder material.

14. A semiconductor package substantially as herein described above and/or as illustrated with reference to Figures 2 to 4 and 15 of the accompanying drawings.

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Application No:	GB 0329351.1	**Examiner:**	Claire Williams
Claims searched:	all	**Date of search:**	31 March 2004

Patents Act 1977 : Search Report under Section 17

Documents considered to be relevant:

Category	Relevant to claims	Identity of document and passage or figure of particular relevance	
X	1, 2, 4, 5, 7, 8, 9, 10, 12, 13	US 2003/0081392 A1	(Cady et al) see paragraphs 0015, 0034 and 0039 and Figure 1
X	1, 2, 5, 7, 8, 9, 10, 12, 13	US 6165817	(Akram et al) see Figure 4
X	1-3, 5	US 6376907 B1	(Takano et al) see whole document

Categories:

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
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Field of Search:

Search of GB, EP, WO & US patent documents classified in the following areas of the UKC[W]:

Worldwide search of patent documents classified in the following areas of the IPC[7]:

H01L

The following online and other databases have been used in the preparation of this search report:

EPODOC, JAPIO, WPI

ABSTRACT

IMPROVEMENTS IN OR RELATING TO ELECTRONICS PACKAGING

The invention provides a mounting for a printed circuit board, ~~which~~ The mounting is suitable for receiving a semiconductor assembly, ~~wherein the mounting comprises:~~

~~A~~ base support 52 ~~having~~ has a semiconductor assembly facing surface, and an opposed printed surface board facing surface;

~~A~~ cover 60 ~~having~~ has a semiconductor assembly facing surface, and an opposed heat radiating surface;

~~A~~ connecting formation 70 which joins the cover to the base support ~~and~~ provides an electrical and thermal communication between the cover and the base support, ~~wherein~~ The connecting formation 70 has a semiconductor assembly facing surface, an outer opposed surface and a thickness between the two surfaces; ~~and~~

~~A~~ plurality of package connectors 54 extending from the base support 52 each of ~~which~~ the package connectors 54 have a printed surface board facing surface; ~~An array of mountings; and~~ ~~A~~ semiconductor package ~~comprising~~ comprises a semiconductor assembly having one or more semiconductor chips, ~~which~~ the assembly is mounted on the mounting wherein the package connectors of the mounting are in a spaced relationship with the base support and are linked electrically with the semiconductor assembly and the cover is arranged to be in a spaced parallel relationship with the base support.

Preferably, the connecting formation has a folding means which comprises a scored line and/or an etched line.

~~(Figure 2 to accompany abstract)~~

figure 12

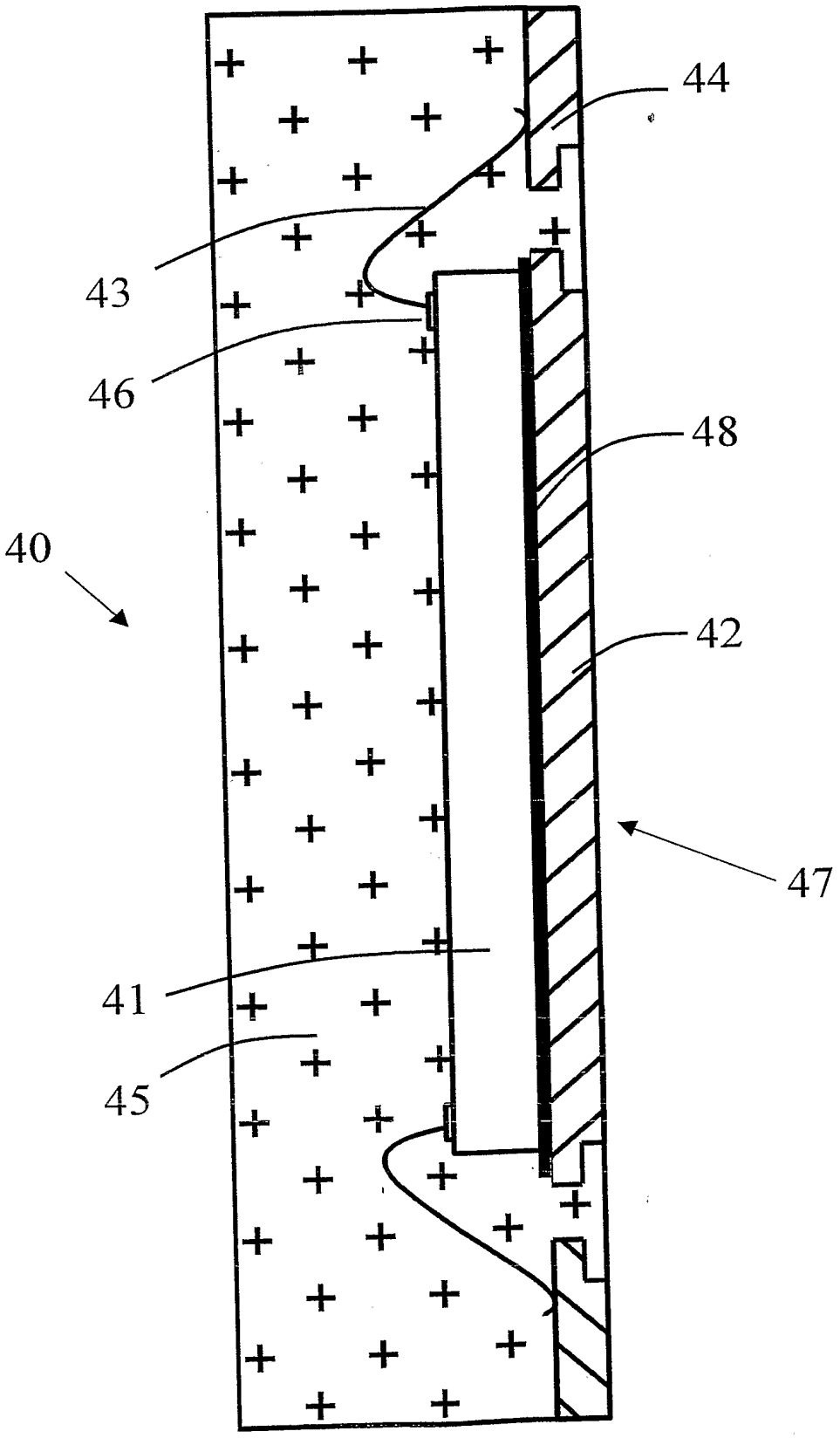


Figure 1

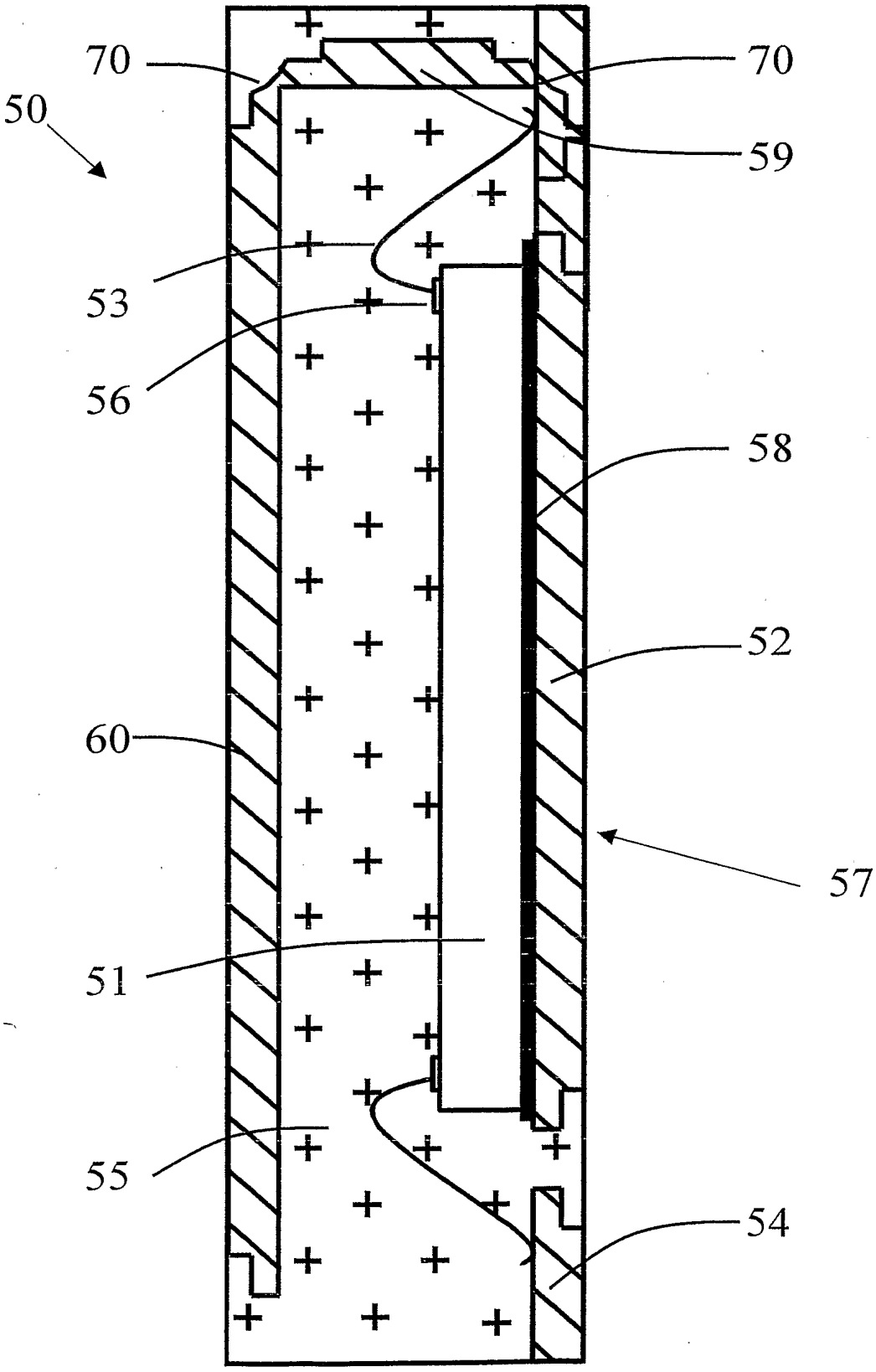


Figure 2

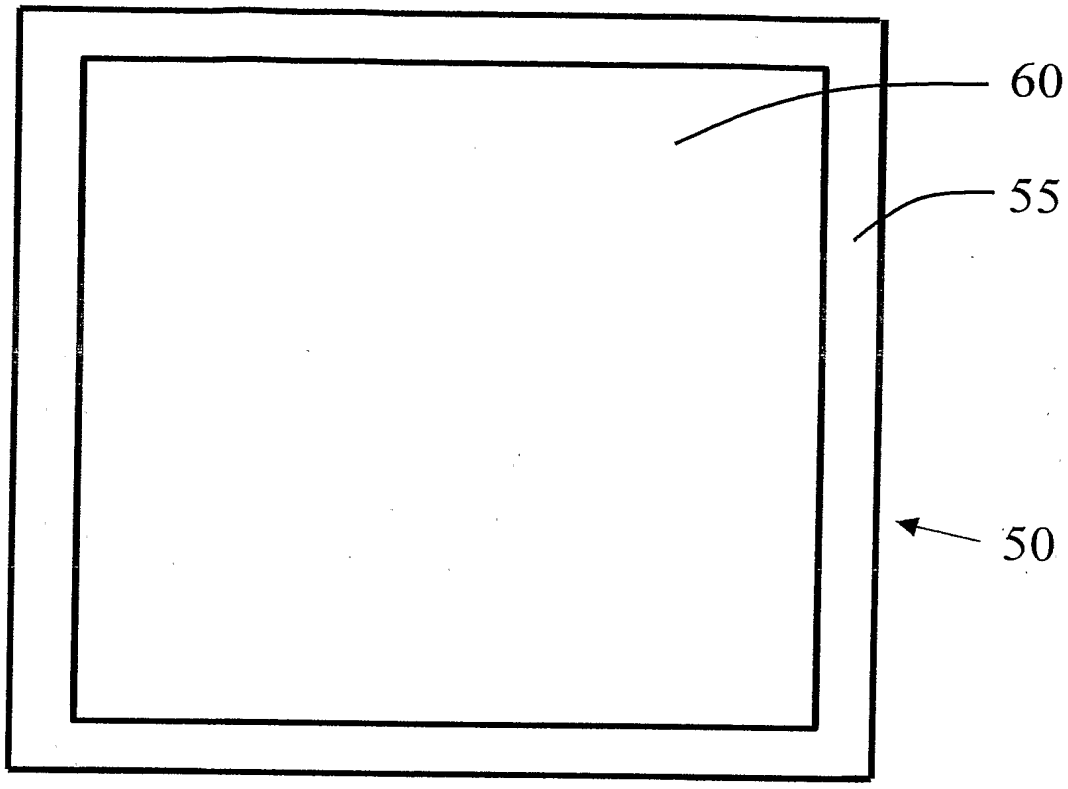


Figure 3

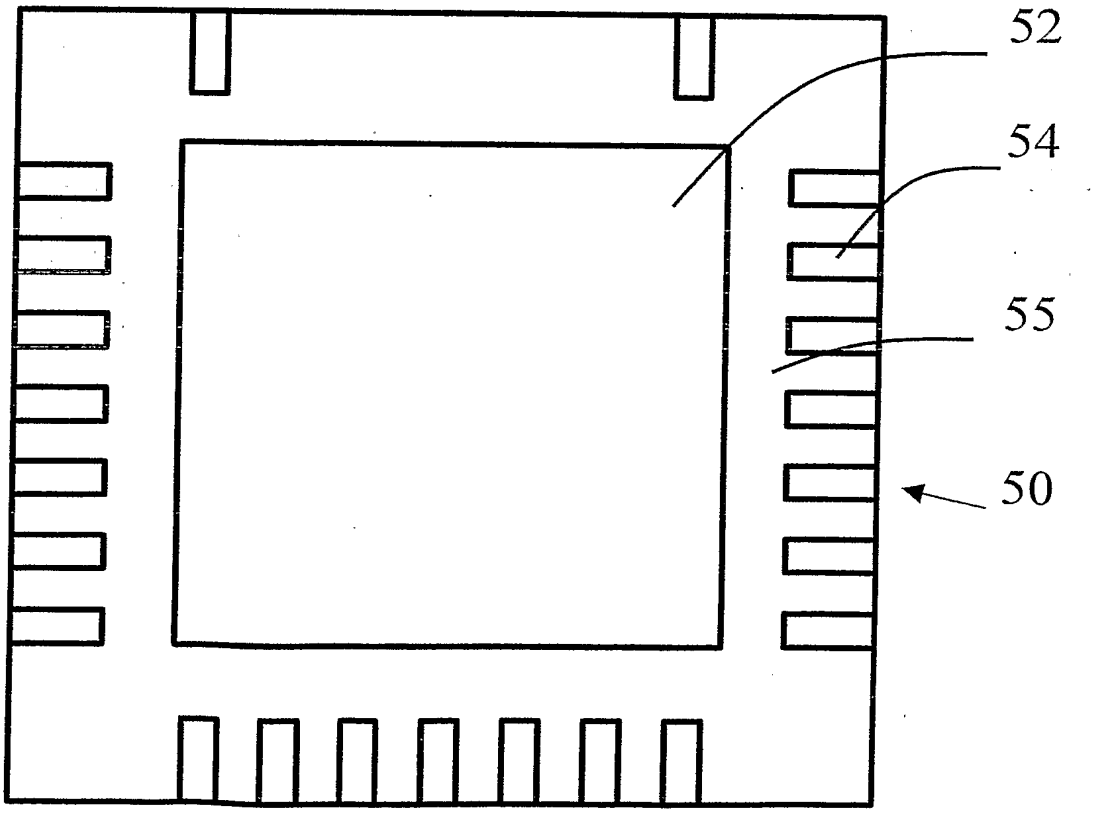


Figure 4

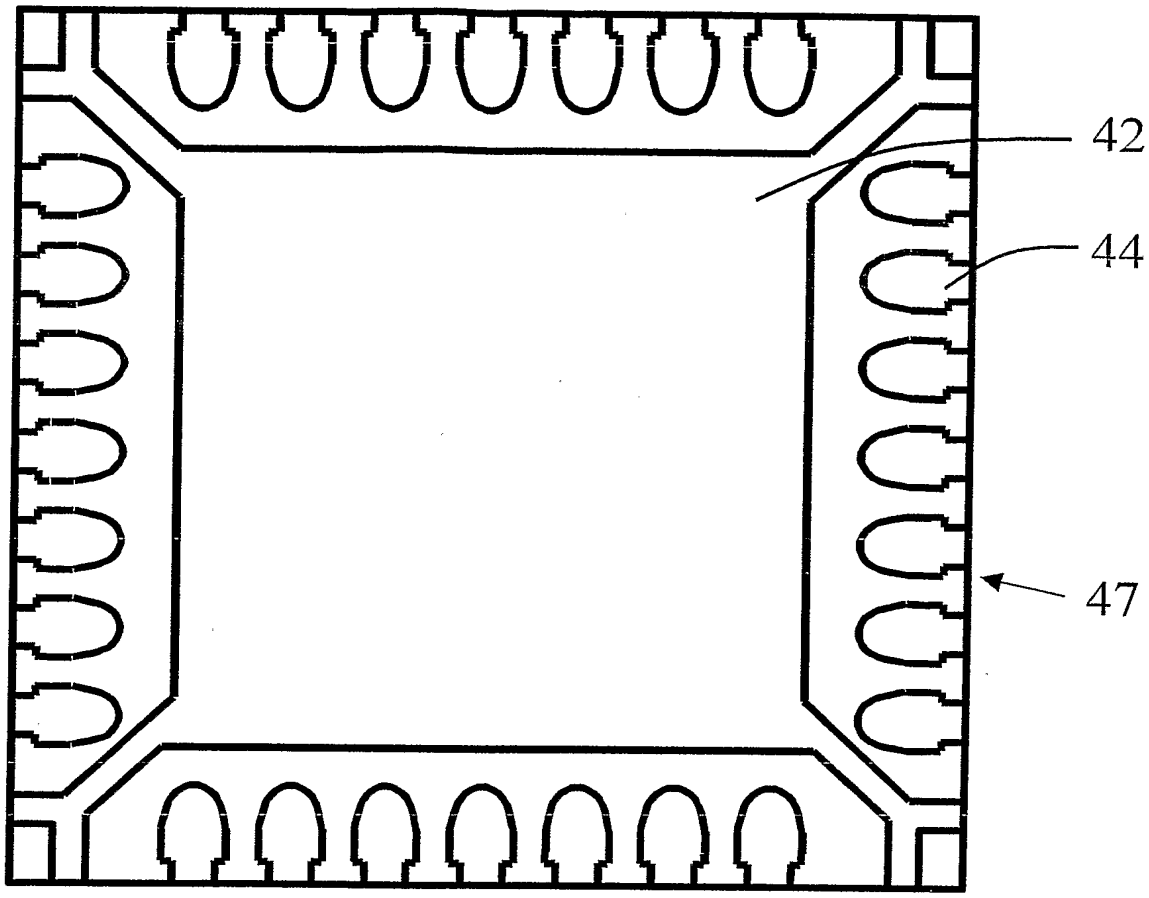


Figure 5

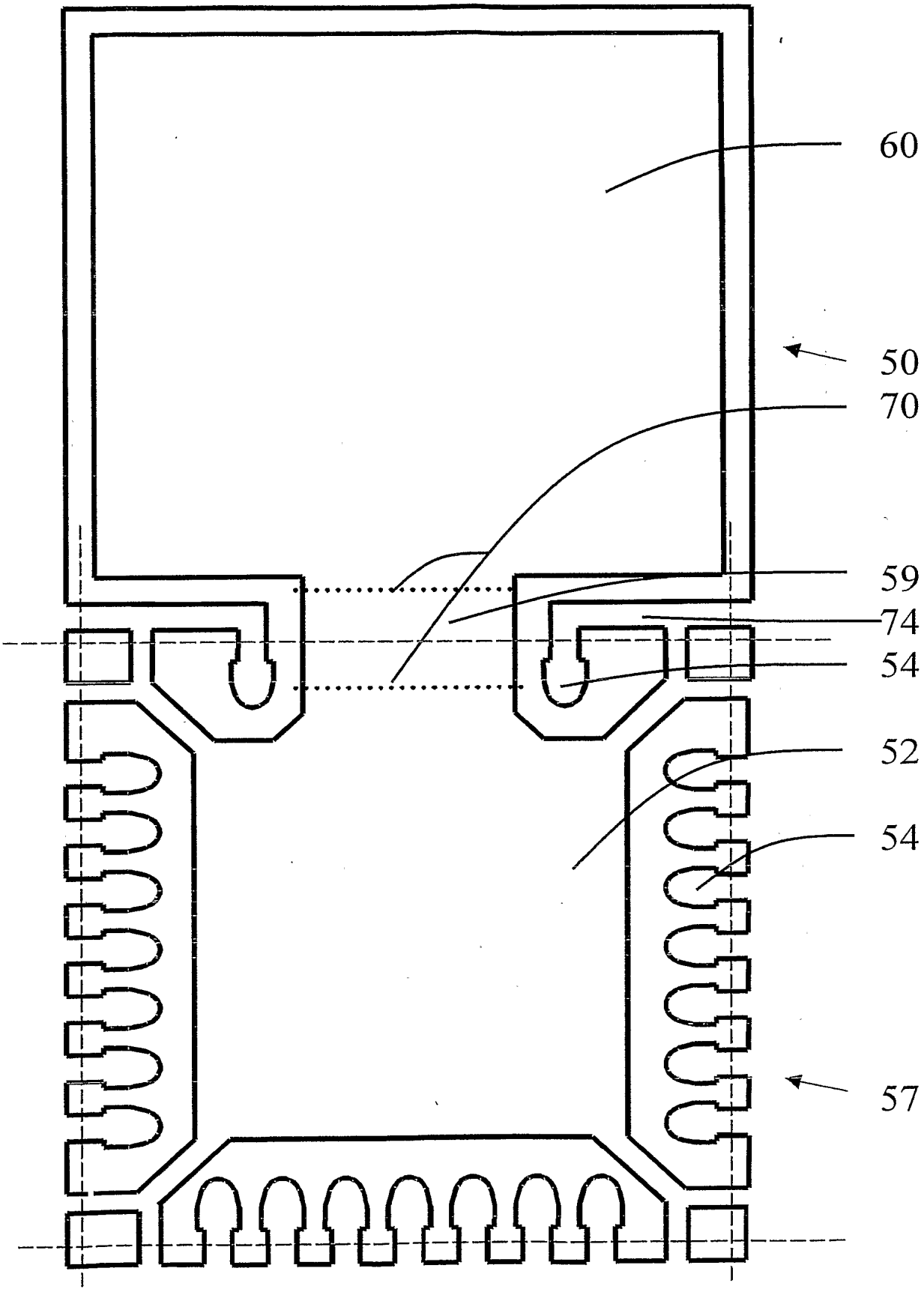


Figure 6

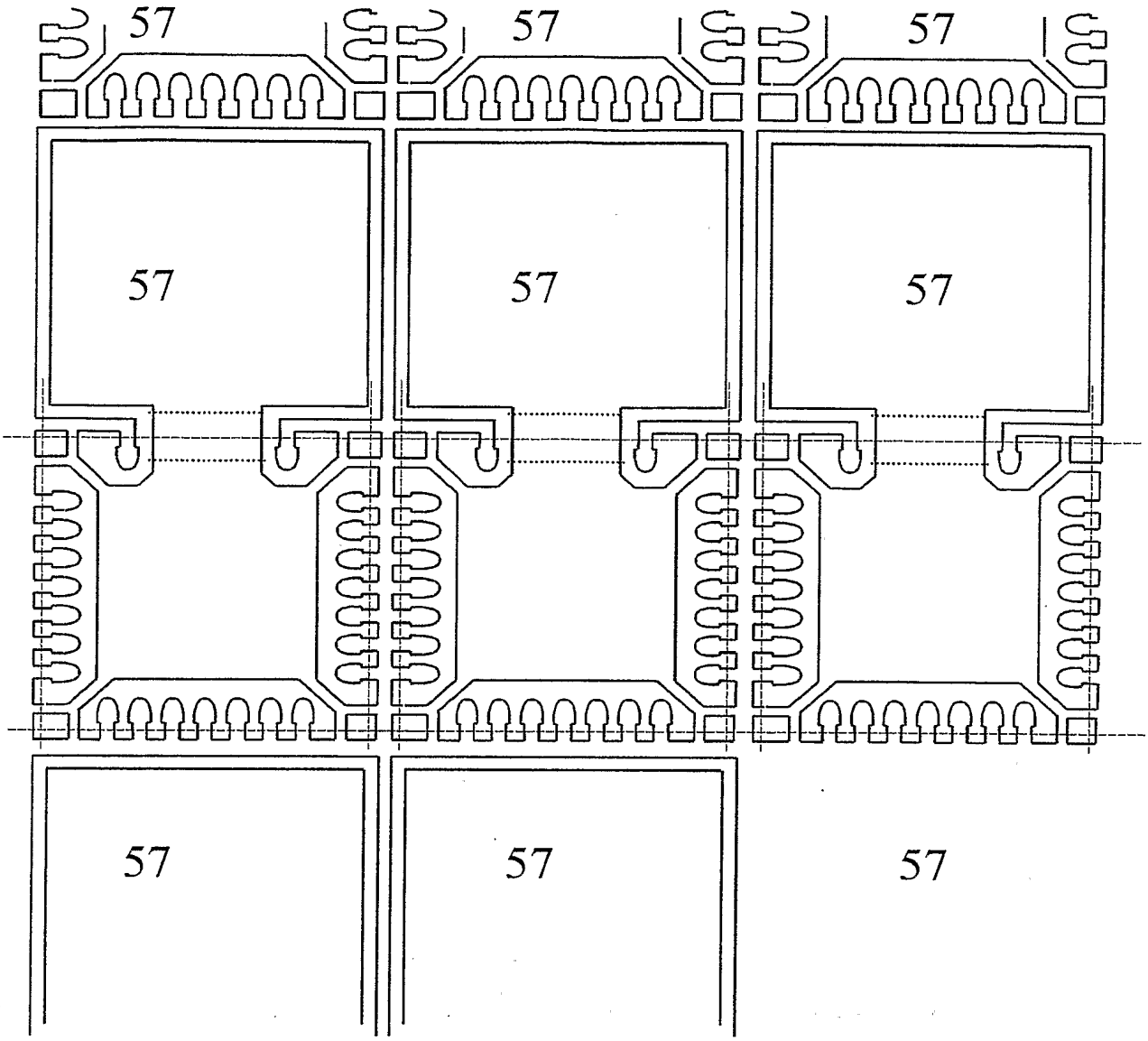


Figure 7

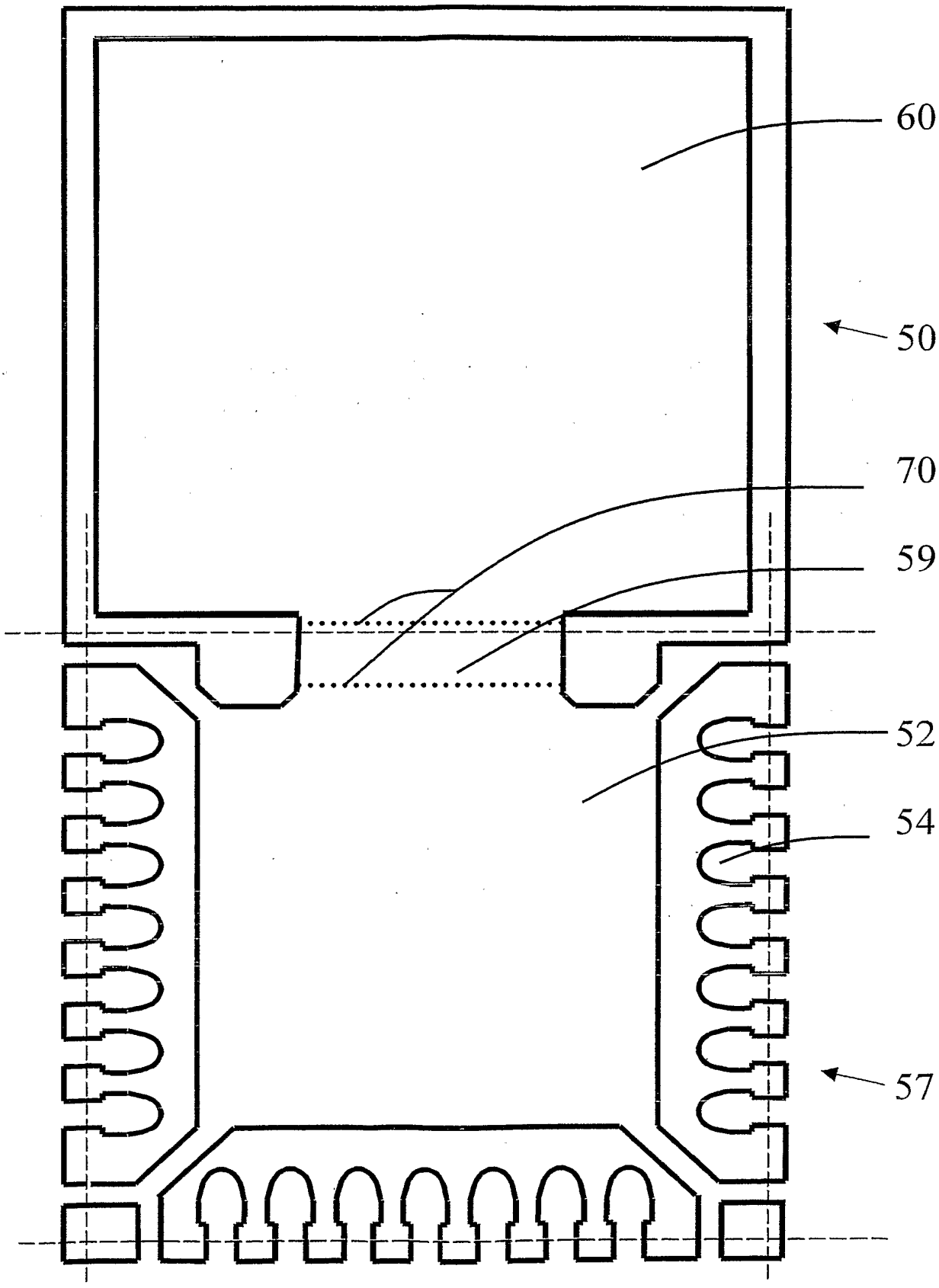


Figure 8

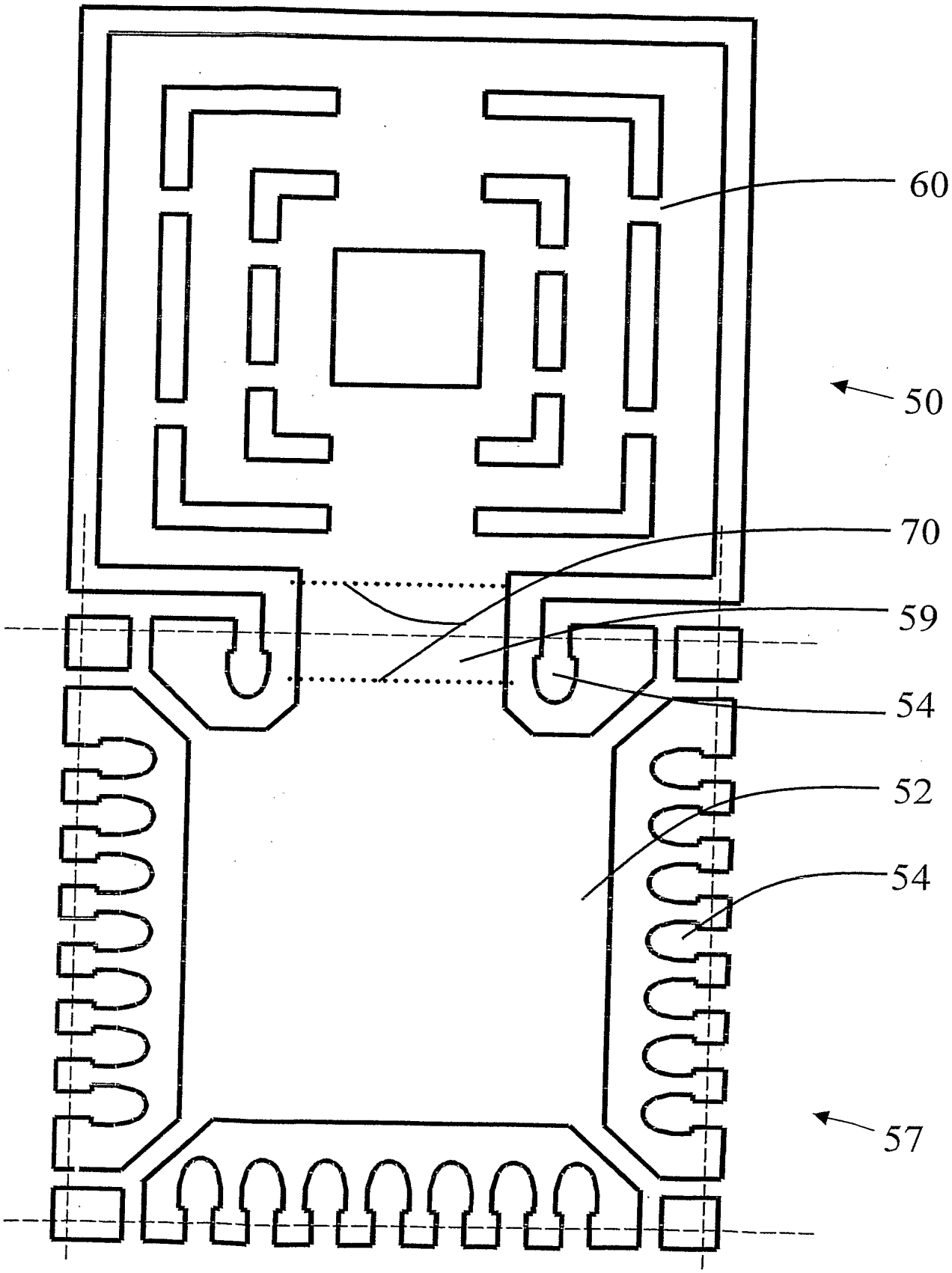


Figure 9

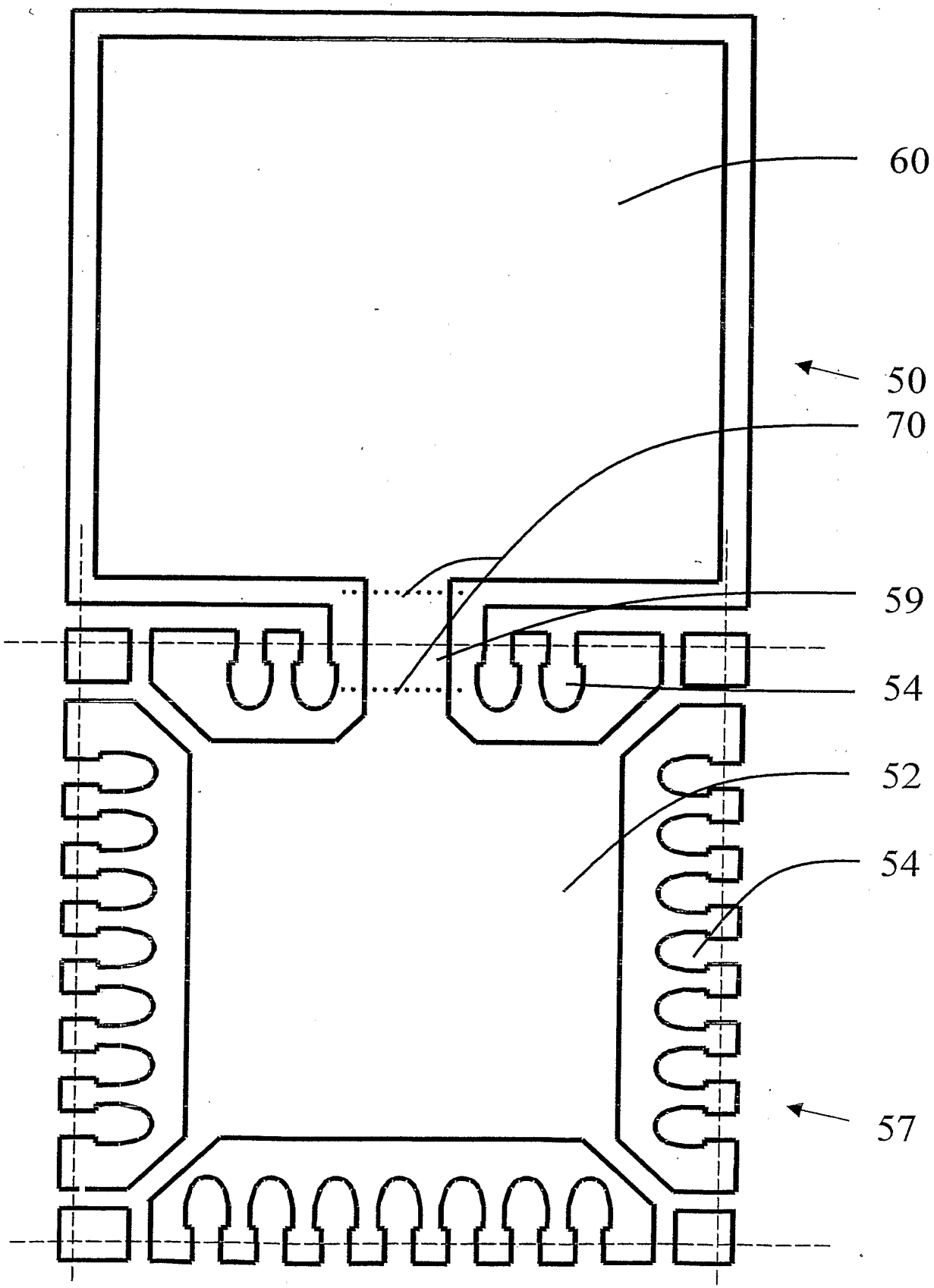


Figure 10

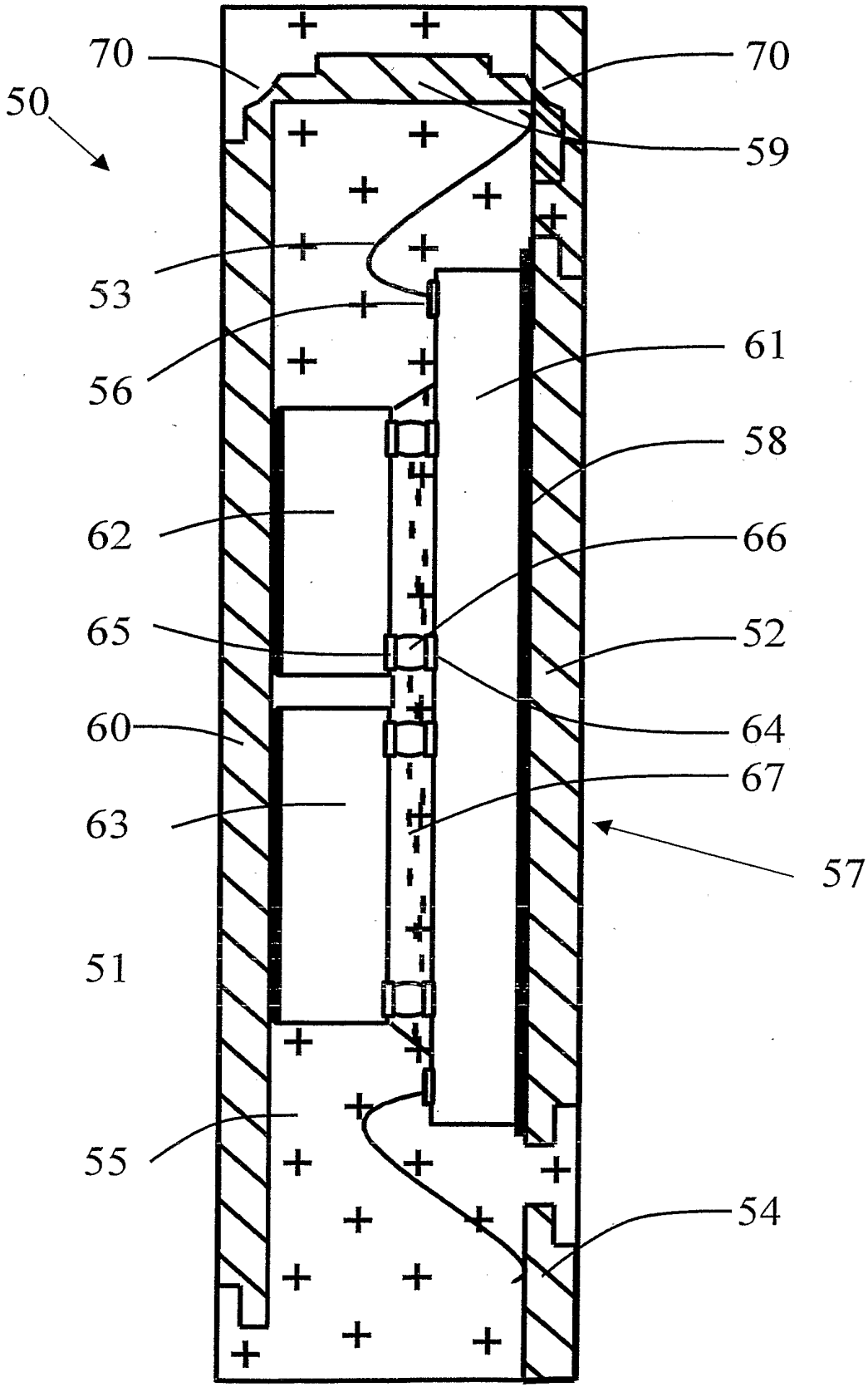


Figure 11

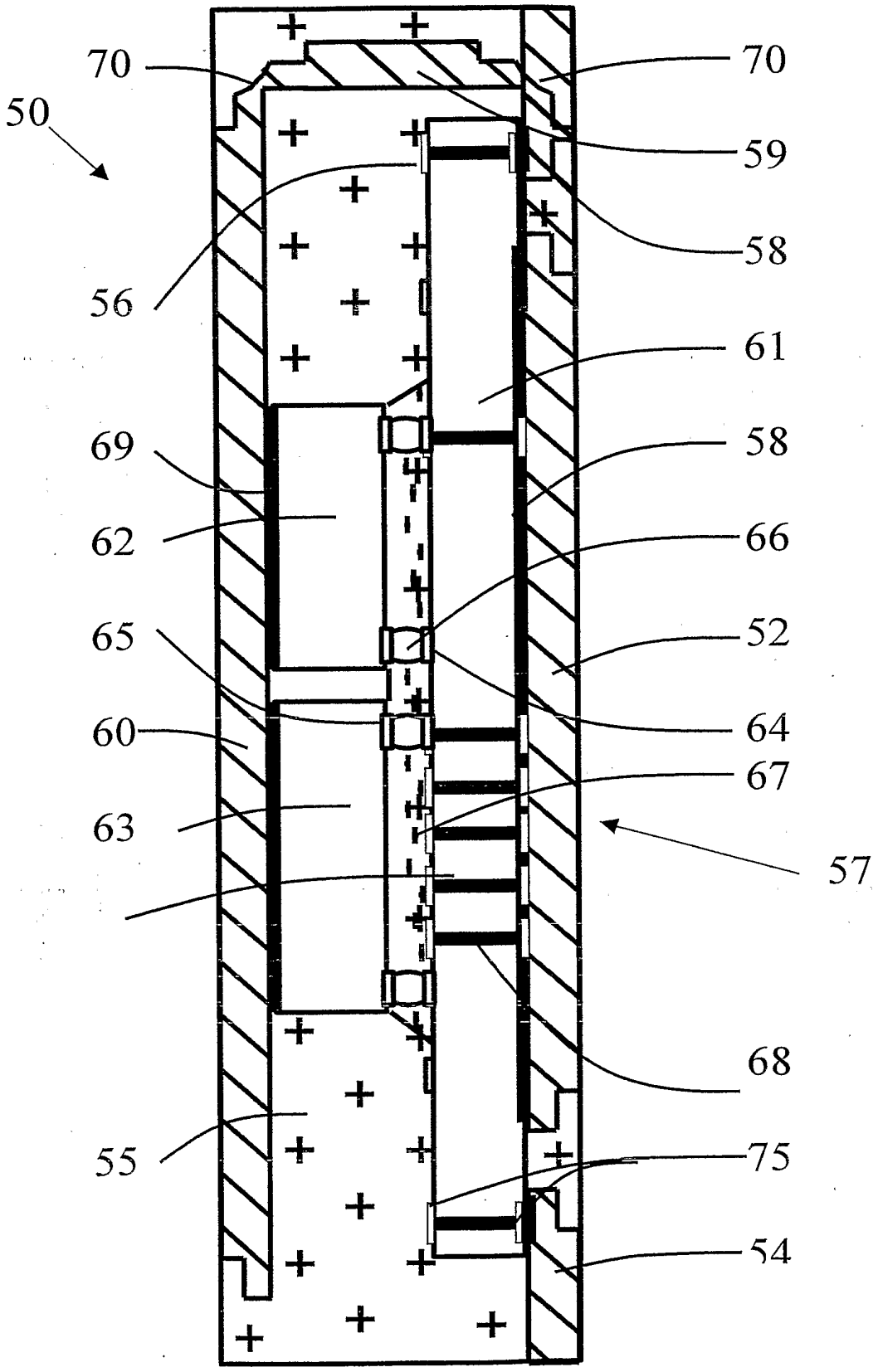
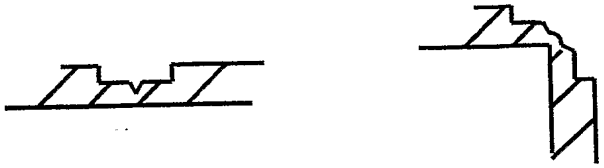
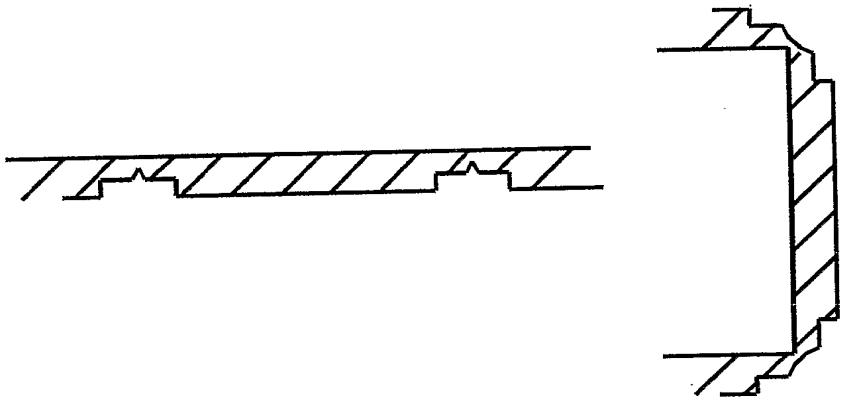


Figure 12



(a) (b)

Figure 13



(a) (b)

Figure 14

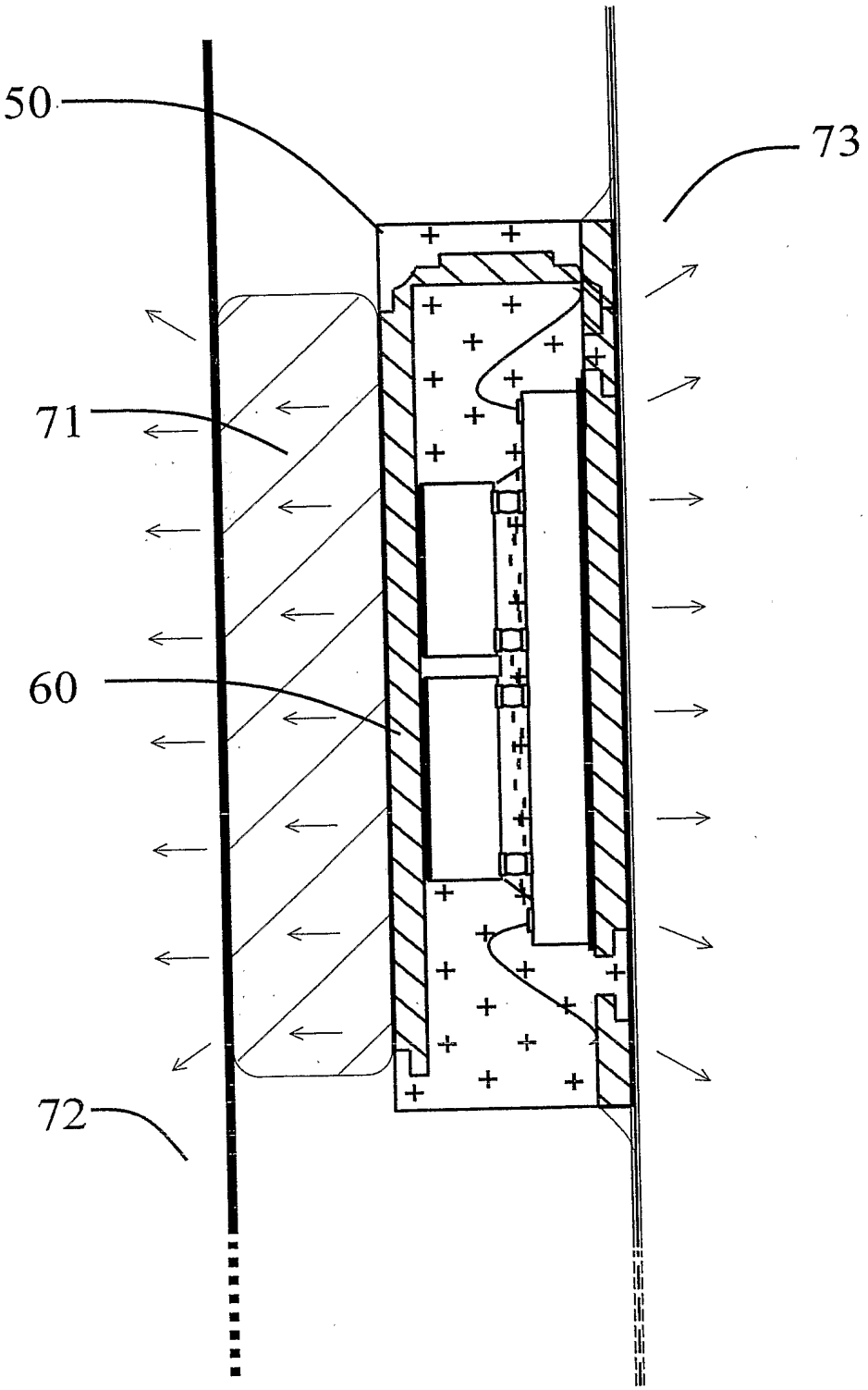


Figure 15